ATTORNEY DOCKET NO. 28951.5186

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Takaki YOSHIDA et al.

Serial No.: 09/697,305

Filed: October 27, 2000

For: FAULT DETECTING METHOD AND LAYOUT METHOD FOR SEMICONDUCTOR INTEGRATED CIRCUIT

Confirmation No.: 4222

Group Art Unit: 2133

Examiner: Joseph D. Torres

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Customer Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Sir:

Prior to the continued examination of the above-identified application, please amend the application as follows: